IN THE ABSTRACT

Please replace the original Abstract with the following substitute Abstract:

A power monitor circuit for notifying processing circuits operating from a first power supply (VDD) that a second power supply (VDDIO) is powered up. VDDIO is greater than VDD. The power monitor circuit comprises: 1) a voltage divider circuit coupled between the second power supply and ground having an output node that goes high when the second power supply is powered up; and 2) an odd number of serially connected inverters operating from the first power supply. An input of a first serially connected inverter is connected to the voltage divider circuit output node. An output of the last serially connected inverter produces a status signal that is the inverse of the voltage divider circuit output node. The status signal is an input to the voltage divider circuit that minimizes the voltage divider circuit's current consumption when the second power supply is ON, while maintaining the status signal value.